



# ASML

## EUV imaging performance and challenges of 10nm and 7nm node Logic

ASML Netherlands: Eelco van Setten, Eleni Psara, Dorothe Oorschot, Erik Wang, Guido Schiffelers, Jo Finders

ASML Brion: Laurent Depre

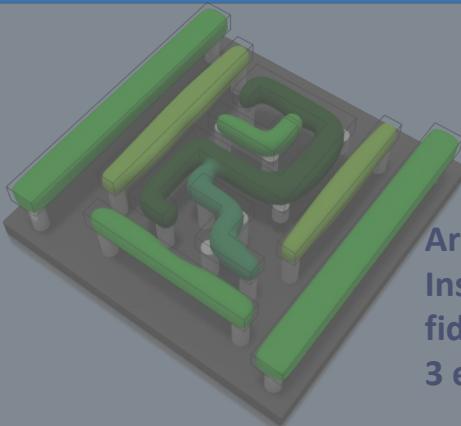
ST Microelectronics: Vincent Farys

# Chipmakers are evaluating patterning solutions for coming Logic nodes

ArFi

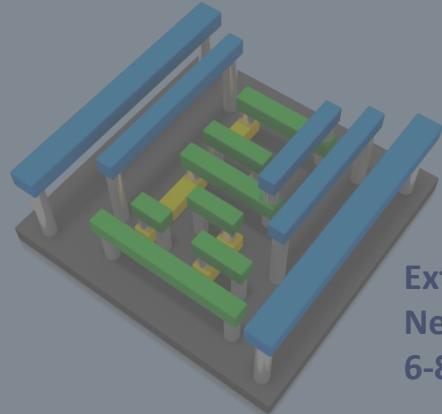
EUV

2D - Single layer solution



ArFi multiple patterning  
Insufficient pattern fidelity  
3 exposures

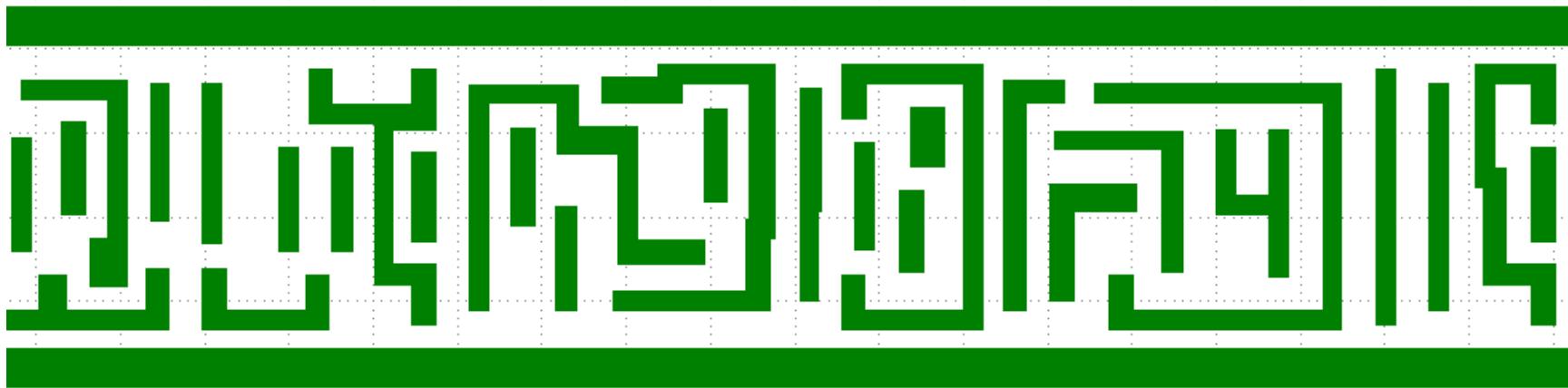
1D - 2-3 layers required



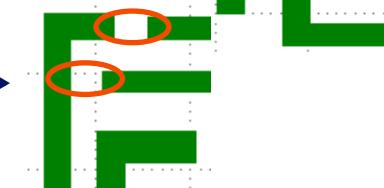
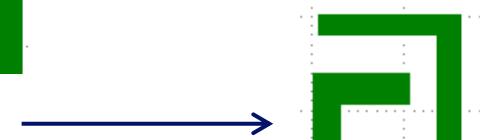
Extra layers needed  
New integration scheme  
6-8 exposures

Good pattern fidelity  
Re-use existing designs  
Single exposure

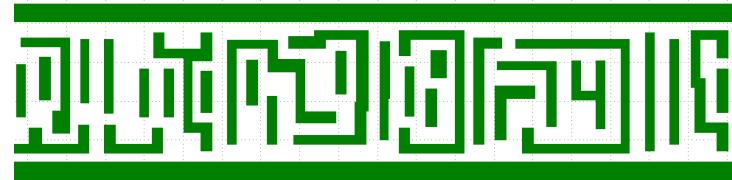
# Logic M1 one of most challenging layers for lithography



- Tightest pitch in design with lines from fully dense to (semi-)iso
- 2D feature shapes (H and V combined), like elbows
- Many line-end features, like tip-to-tip and tip-to-space

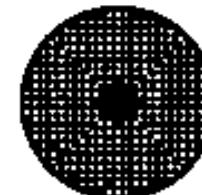


# Logic M1 evaluated on ASML's NXE:3300B using conventional and Quasar illumination at low dose



	NXE:3300B
NA	0.33
Illumination	Conventional 0.9σ, 6 off-axis pupil settings
Resolution	22 nm
Dedicated Chuck Overlay / Matched Machine Overlay	3.0 nm / 5.0 nm
Productivity	55 - 125 Wafers / hour
Resist Dose	15 mJ/cm <sup>2</sup>

	Logic M1 – 10nm node
Min. pitch	~ 42 – 48nm
CD control	~ 1.4-1.7nm (7% min. HP)
Min. Tip-to-tip	~35-50nm
Min. Tip-to-space	~28-35nm

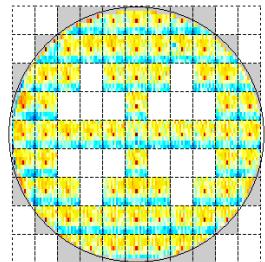


# Contents

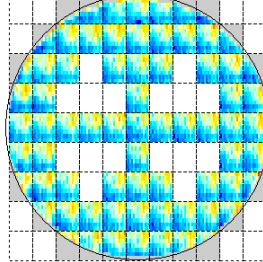
- **NXE:3300B imaging performance – Building blocks**
  - *CDU, HV, through pitch and full lot performance from scanner qualification*
  - *Line end control*
- 2D random logic – 10nm node Metal 1
  - *OPC model calibration and hotspot verification*
- Towards 7nm node logic
- Summary and conclusions

# Multiple NXE:3300B systems show CDU below 1.5nm dense and iso lines exposed at 16mJ/cm<sup>2</sup> – conventional ill.

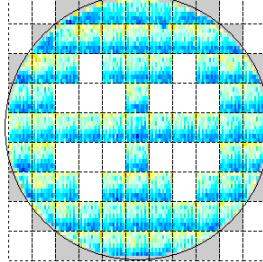
System A



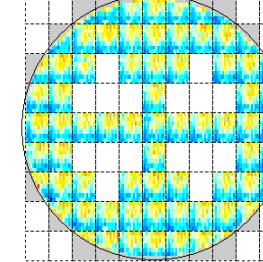
System B



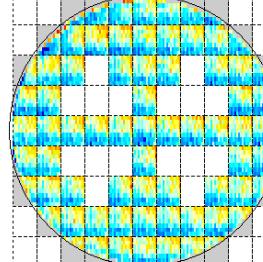
System C



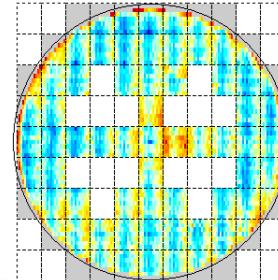
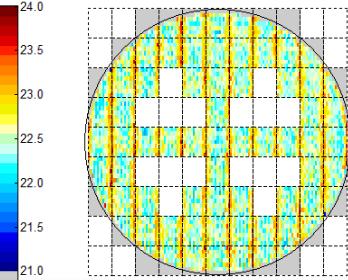
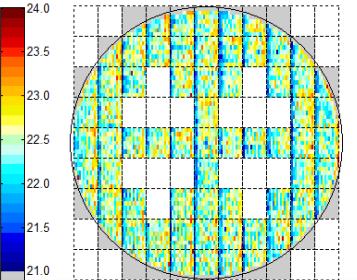
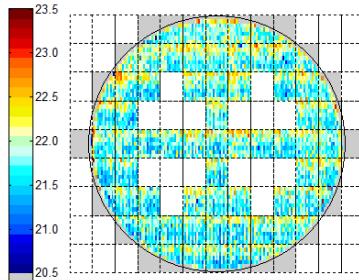
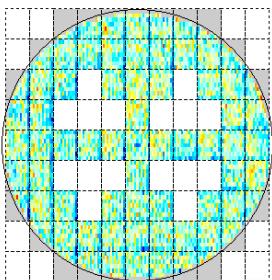
System D



System E



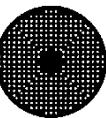
22nm DLs: Full wafer CDU <1.2nm



22nm ILs: Full wafer CDU < 1.5nm

Data corrected for reticle errors and mask shadowing effect

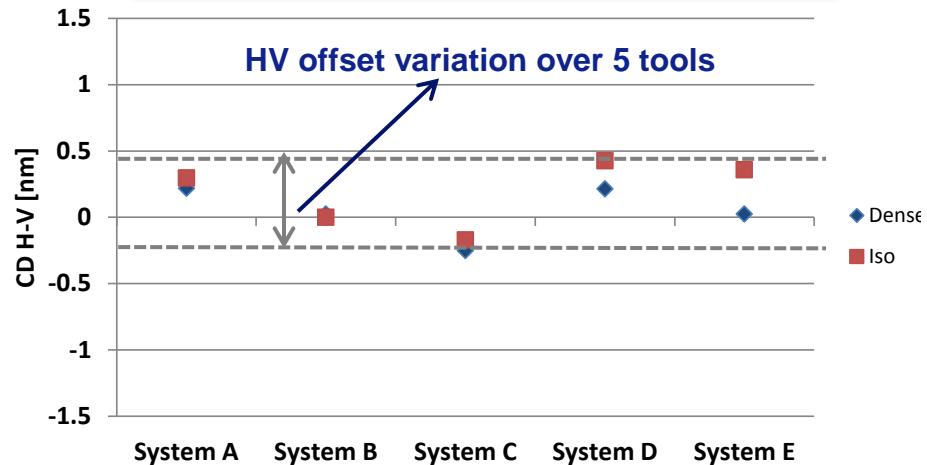
CD measurements performed with YieldStar



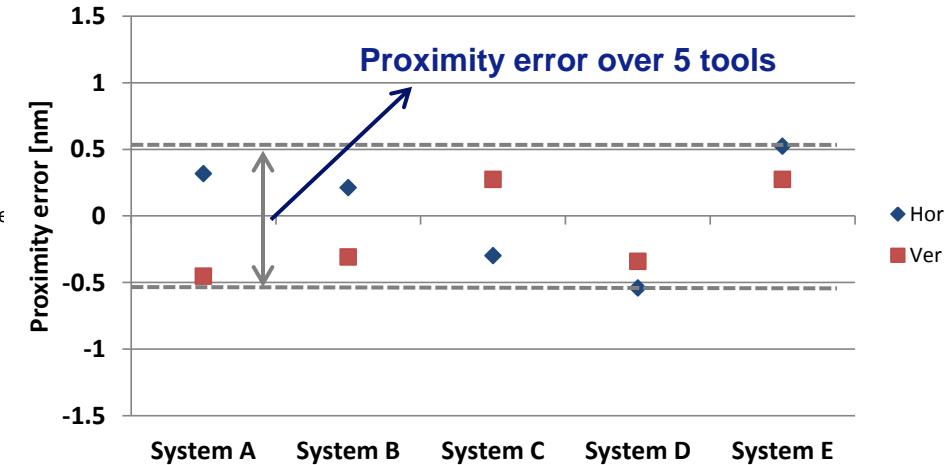
# NXE:3300B shows stable HV offset and CD through pitch control between systems

- HV offset variation over 5 tools within +/-0.35nm
- CD through pitch control over 5 tools within +/-0.55nm (< +/- 3% TargetCD)

22nm dense and iso lines HV offset stability



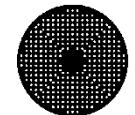
22nm H&V L/S through pitch stability



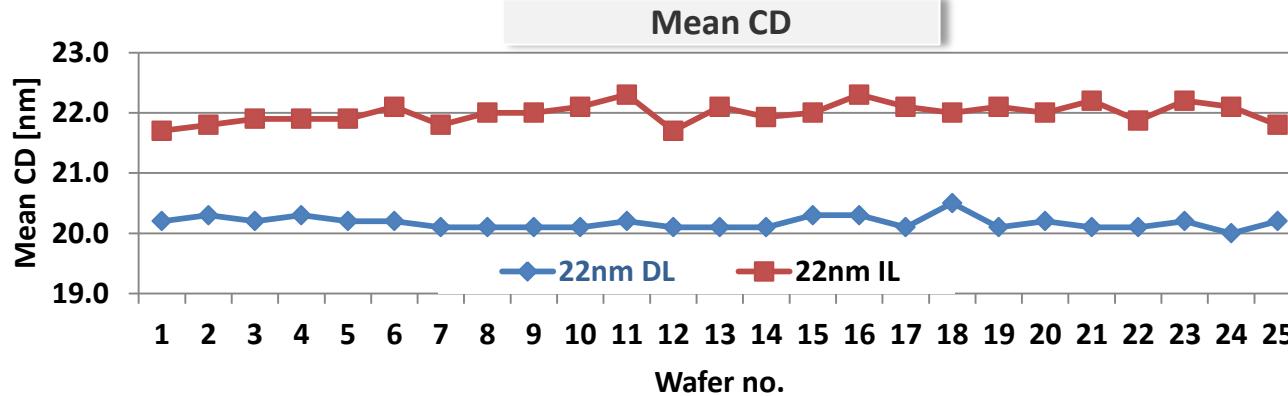
22nm H and V L/S,  
pitch 44 and 154nm

Reference pitch ← 16mJ/cm<sup>2</sup>

22nm L/S, pitch 44, 50.5,  
57, 66, 88 and 154nm



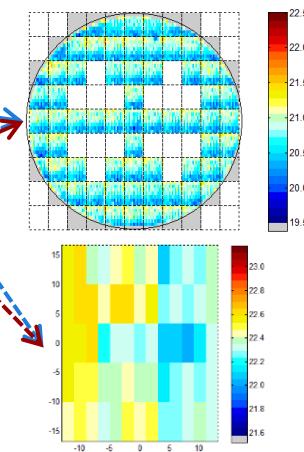
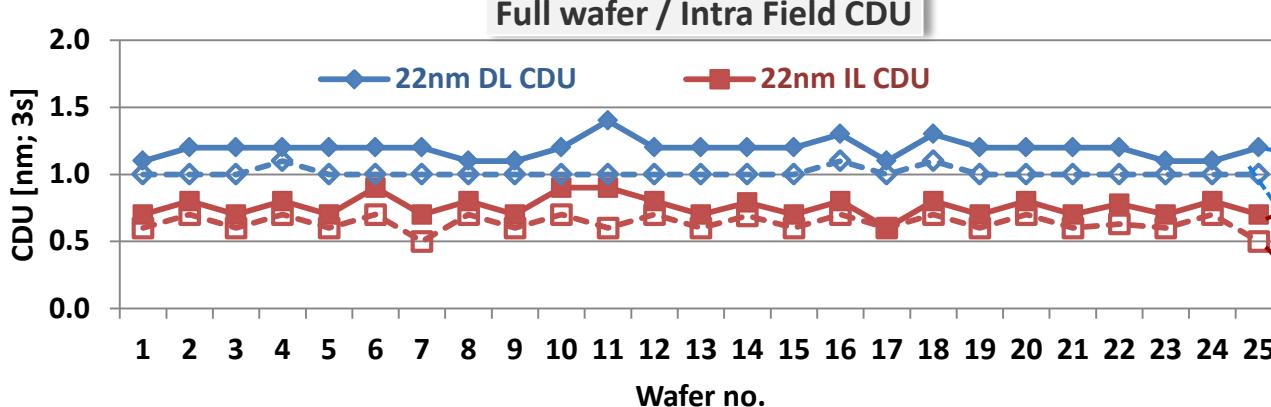
# NXE:3300B shows stable through lot performance



Courtesy of IBM

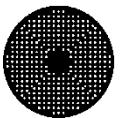
Through lot stability  
(HV pooled data):

- Mean CD: +/- 0.3nm
- FW CDU: +/- 0.15nm
- IF CDU: +/- 0.1nm

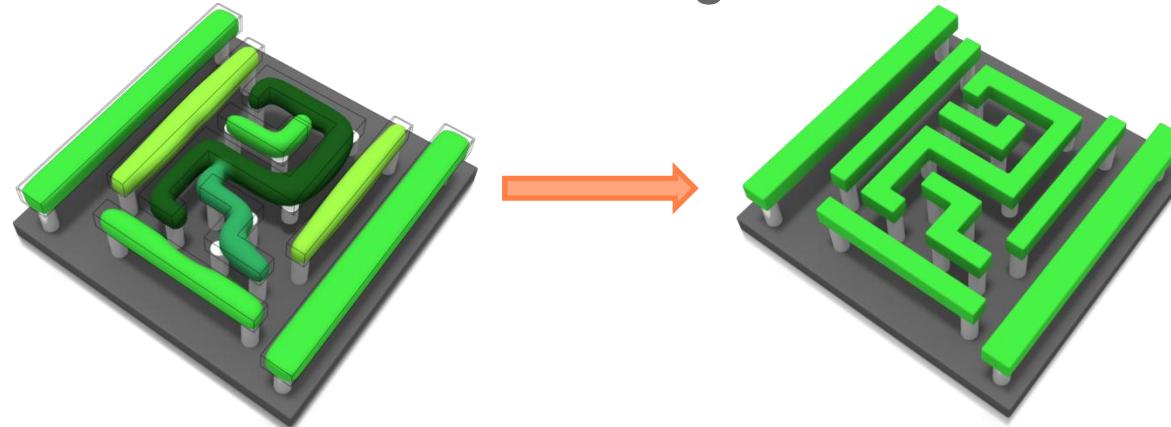


22nm H and V L/S, pitch 44 and 154nm @ 16.6mJ/cm<sup>2</sup>

CD measurements performed with YieldStar



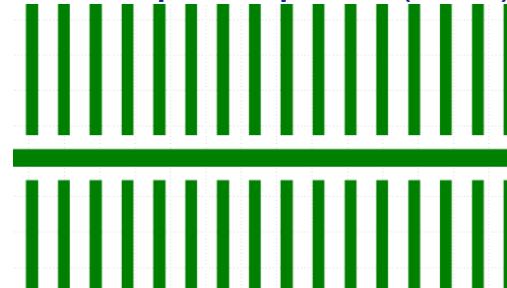
# Good line-end control allows aggressive shrink of random 2D logic



- Line end performance evaluated using dedicated test structures



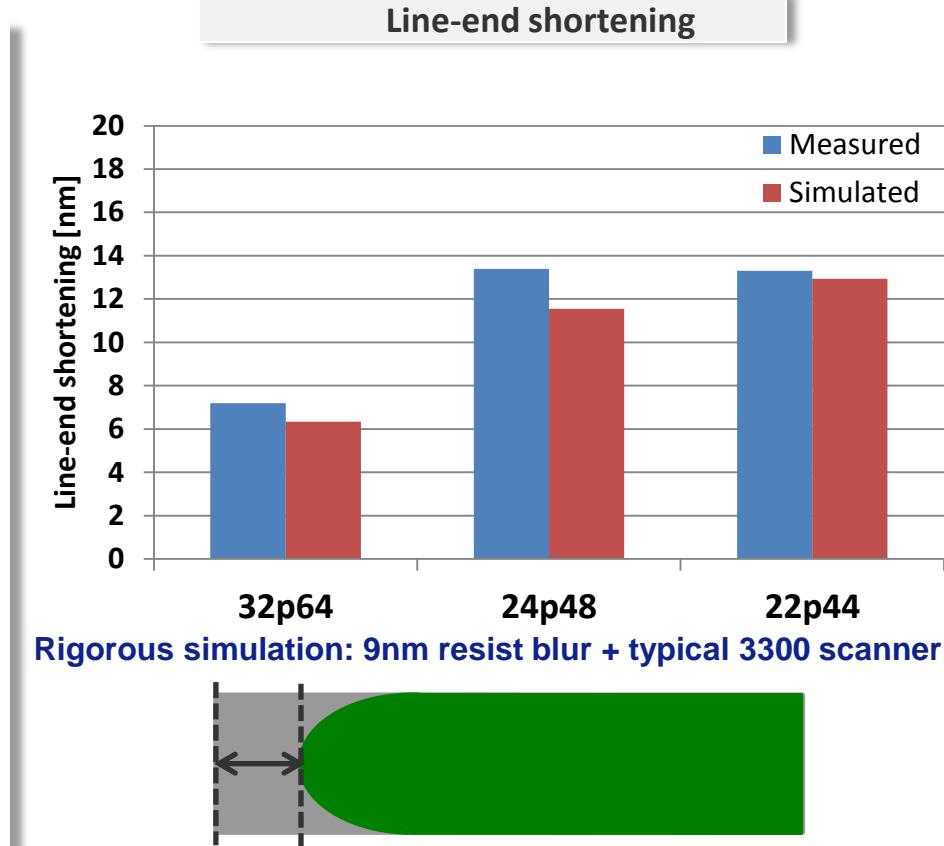
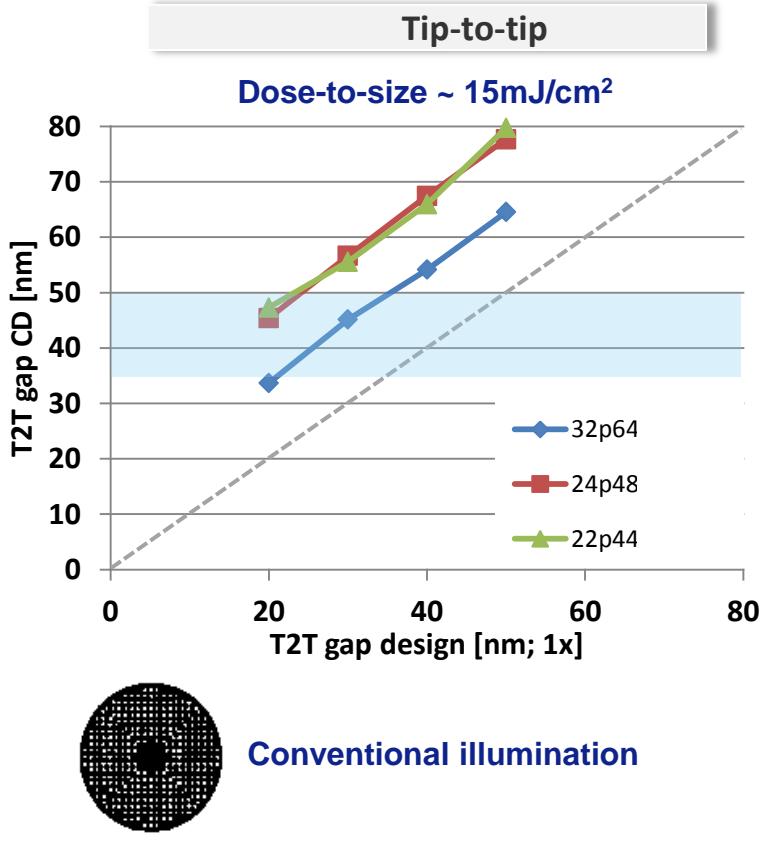
Tip-to-space (T2S)



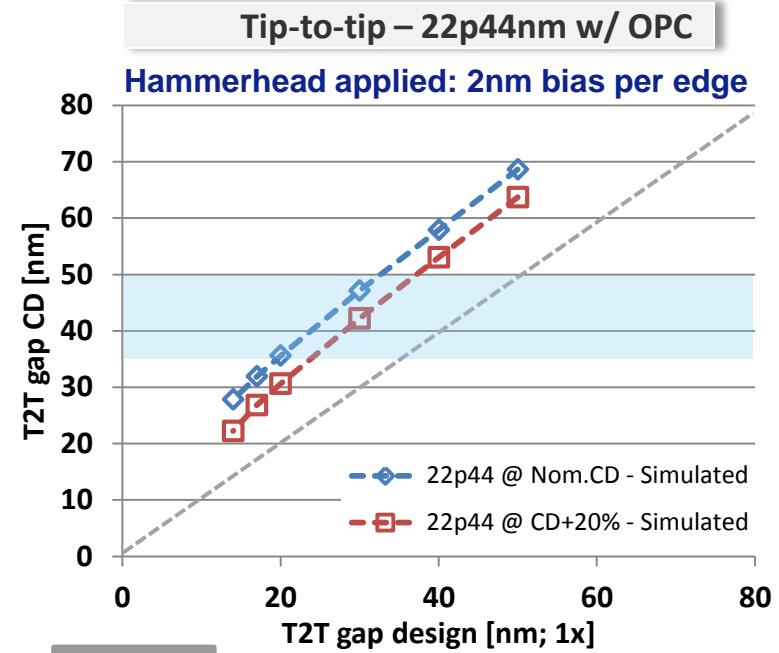
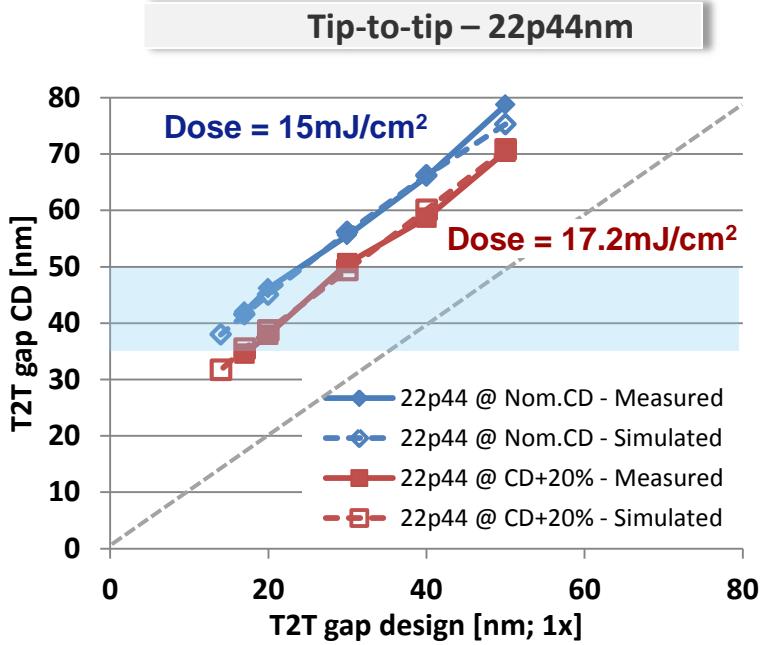
*Dark field pattern → polygon = space*

Logic M1 – 10nm node	
Min. pitch	~ 42 – 48nm
Min. Tip-to-tip	~35-50nm
Min. Tip-to-space	~28-35nm

# Resist shows significant Line-end-shortening of ~ 13nm for 24 and 22nm HP designs



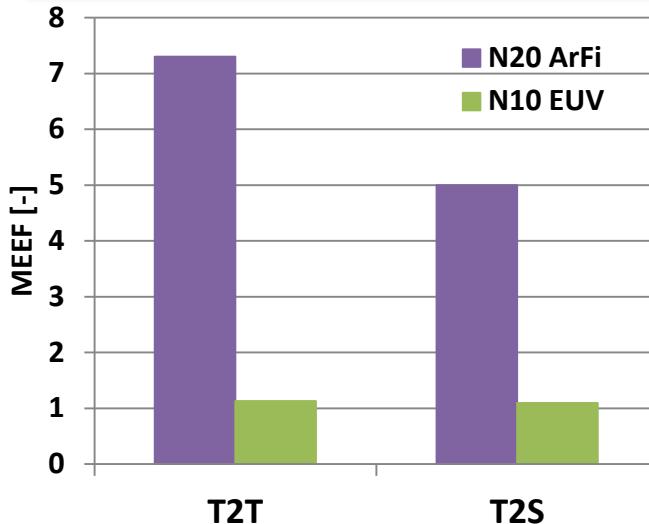
# T2T < 25nm feasible at low dose by means of OPC and overexposure trench



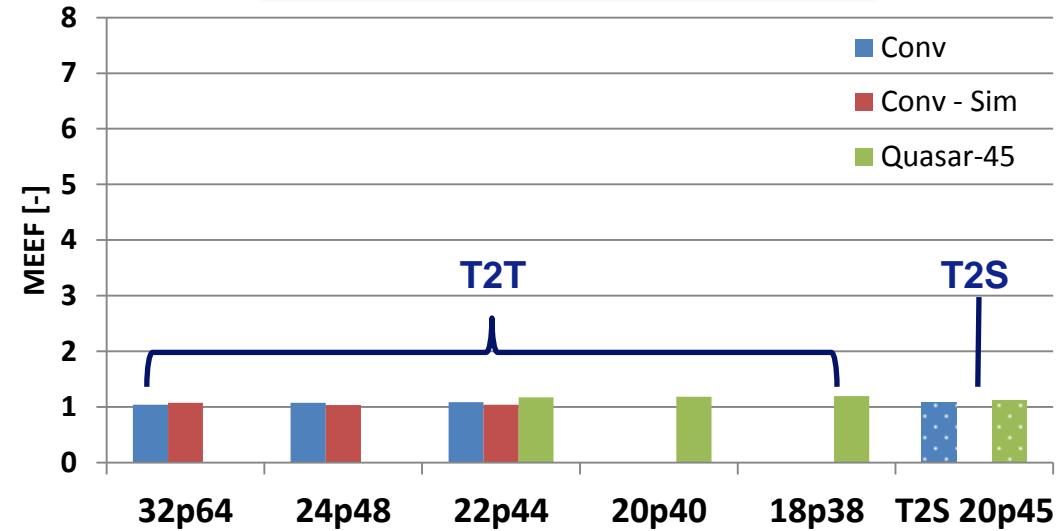
- T2T of 30nm feasible by lowering gap CD on mask to 14nm (1x) and overexposure trench (CD+20%)
- Simulations: OPC (eg. Hammerheads) enables < 25nm T2T at low dose

# MEEF T2T/T2S close to 1 for N10. More than 5x improvement w.r.t. N20 performance with ArFi

T2T and T2S MEEF – N20 ArFi vs N10 EUV

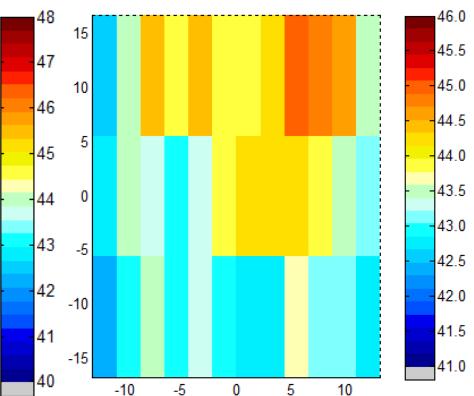
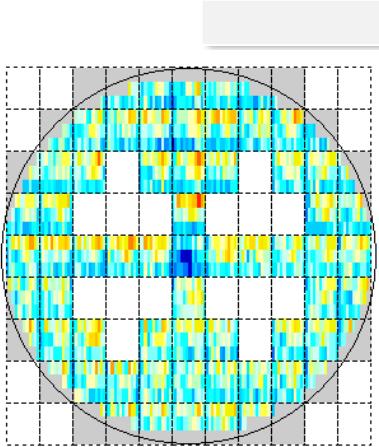
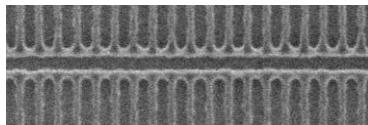
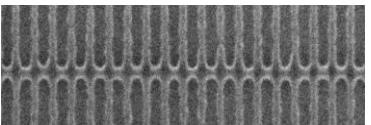


T2T and T2S MEEF – EUV



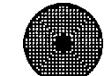
- Low Mask Error Enhancement Factor for gap CD for both T2T and T2S features for various grating pitches
  - Both for Conventional and Quasar illumination, supported by simulations
  - Large improvement w.r.t. current performance at N20 using ArFi

# Raw full wafer CDU T2T and T2S < 7% of targetCD at 18mJ/cm<sup>2</sup>

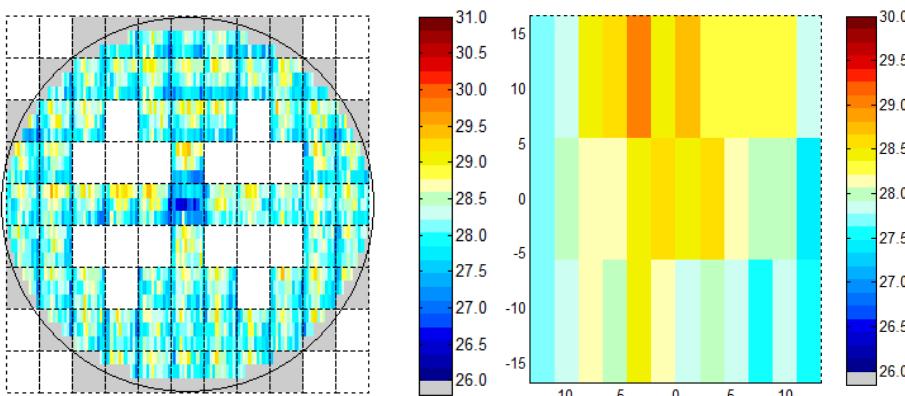
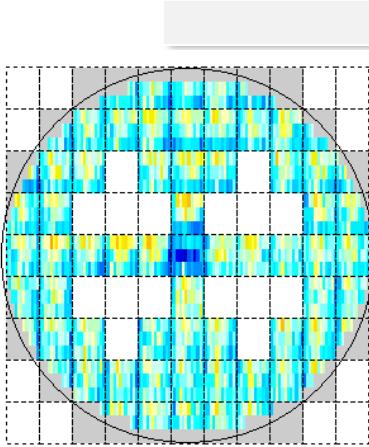


22nm dense L/S with 20nm gap (1x) @ 18mJ/cm<sup>2</sup>

Including reticle fingerprint



T2T CDU	Mean gap CD	FW CDU	IF CDU
V trench	43.6nm	2.6nm	2.0nm
H trench	40.3nm	2.8nm	2.4nm



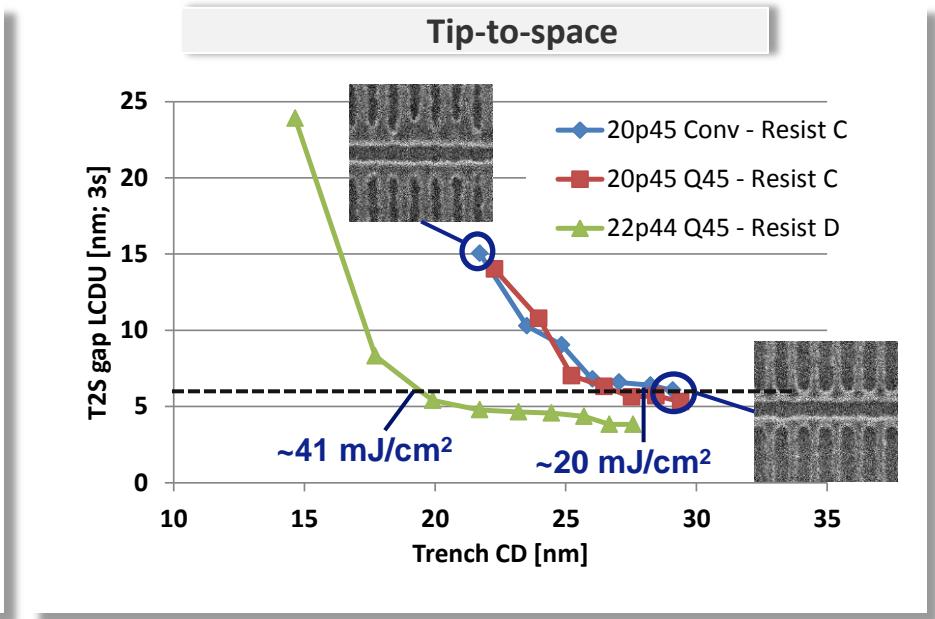
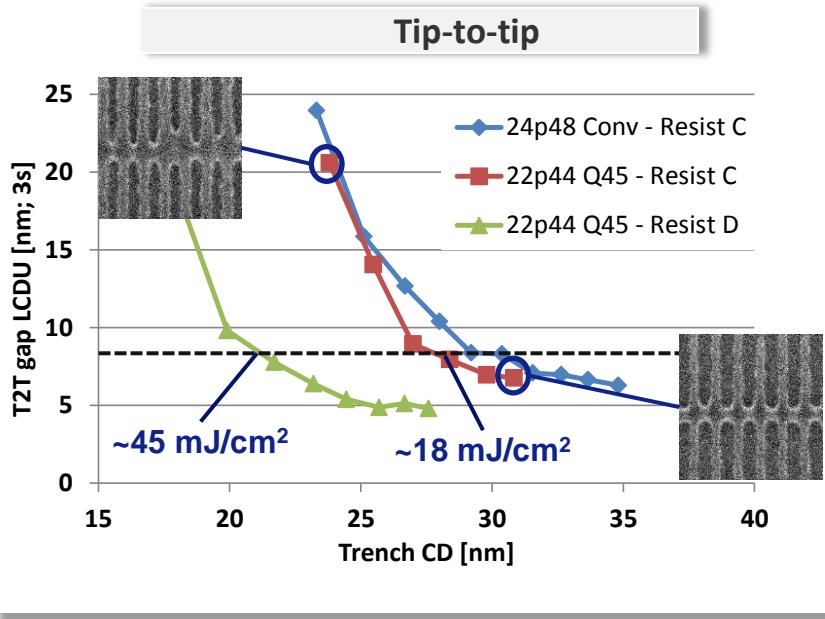
22nm dense L/S with 20nm gap (1x) @ 18mJ/cm<sup>2</sup>

Including reticle fingerprint



T2S CDU	Mean gap CD	FW CDU	IF CDU
V trench	28.1nm	1.4nm	1.1nm
H trench	25.4nm	1.4nm	1.0nm

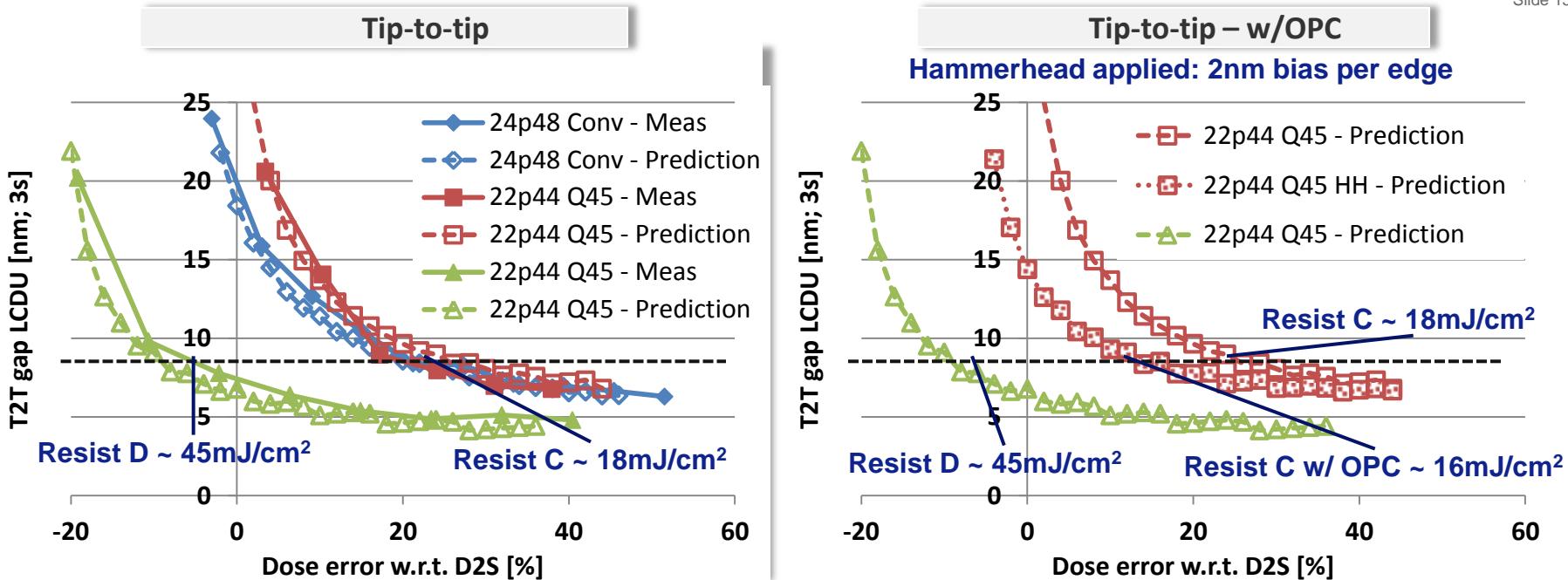
# Local gap CDU dependent on trench width and resist contrast



Logic M1	20nm node ArFi - Actual	10nm node EUV – Scaled from N20
Tip-to-tip LCDU	~11nm	<8nm
Tip-to-space LCDU	~7.5nm	<5.5nm

- Large LCDU at small trench width → More advanced OPC (Hammerheads) expected to reduce LCDU significantly

# Local gap CDU driven by dose sensitivity and resist properties. OPC reduces LCDU



- LCDU prediction:  $LCDU \sim A * D * dCD/dD$ 
  - $A$  = resist dependent constant
- LCDU trend driven by dose sensitivity

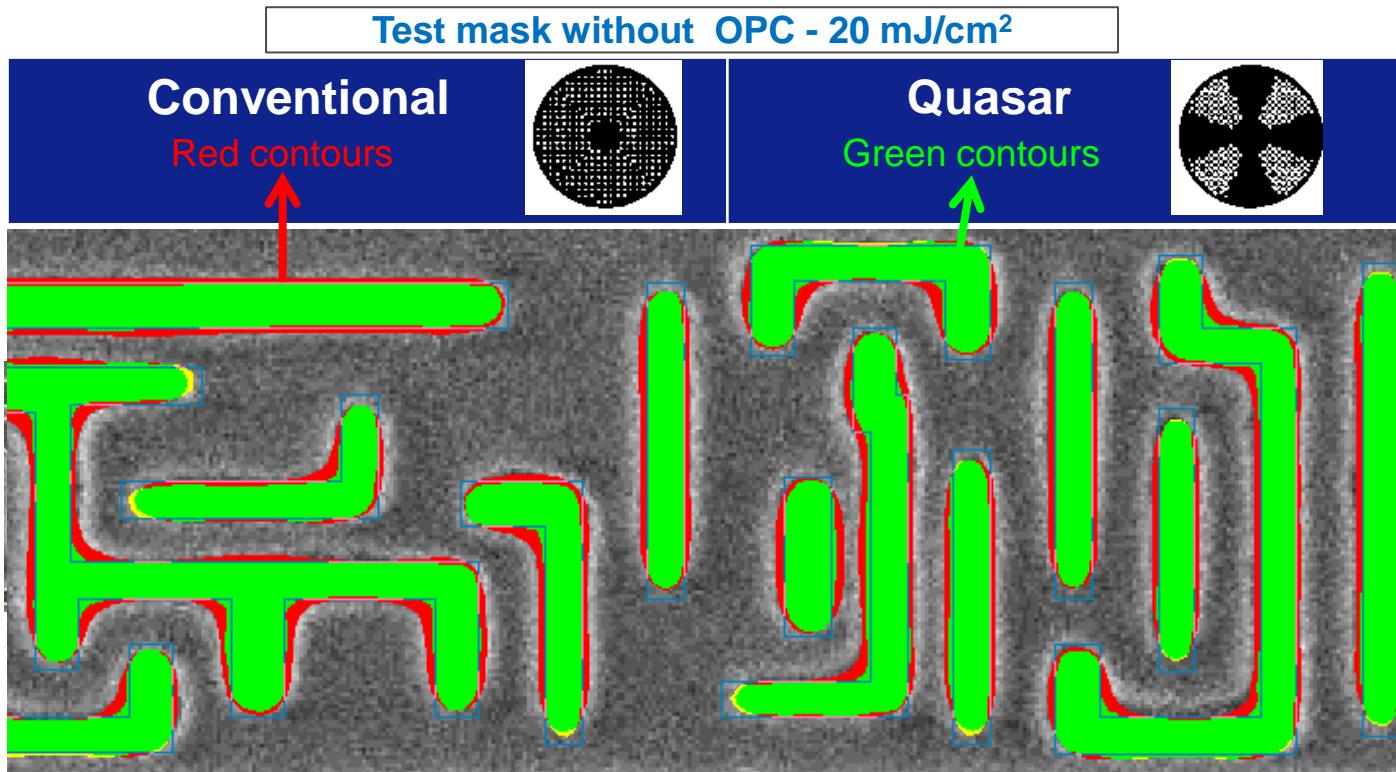
- OPC (Hammerhead) reduces LCDU at same dose or allows dose reduction at same LCDU

# Contents

- NXE:3300B imaging performance – Building blocks
  - *CDU, HV and through pitch performance from scanner qualification*
  - *Line end control*
- **2D random logic – 10nm node Metal 1**
  - *OPC model calibration and hotspot verification*
- Towards 7nm node logic
- Summary and conclusions

# Accurate Metal layer model for multiple illumination modes

## Calibrated Tachyon NXE M3D+ model



- Quasar-45 shows better pattern definition

NXE:3300, 10 nm logic metal 1 layer, 45 nm pitch

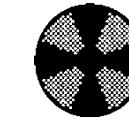
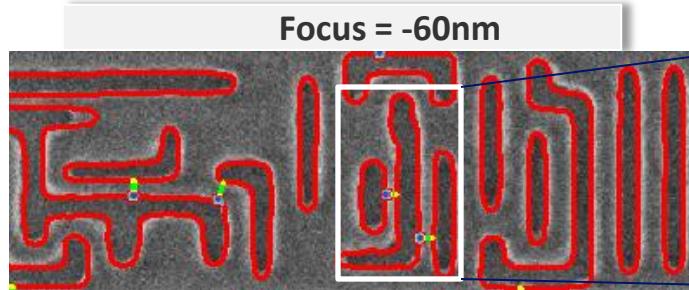
# Tachyon Litho Manufacturing Check (LMC) & M3D+

ASML

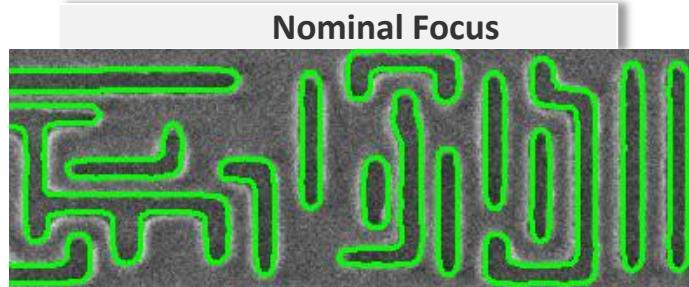
correctly predicts bridge- and neck-defects through focus

Public

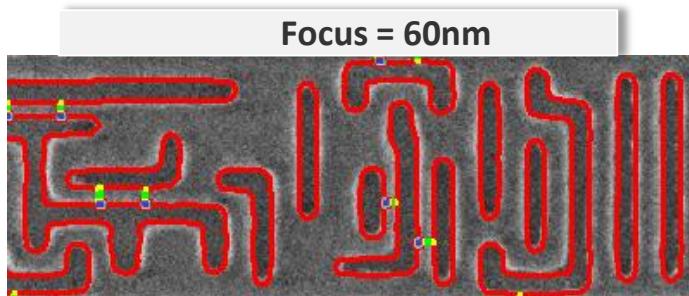
Slide 18



Test mask without OPC  
20 mJ/cm<sup>2</sup>



No bridge- and neck-defects expected at nominal conditions → in line with observations



Potential bridge defects in defocus (+/60nm) highlighted by LMC → in line with observations

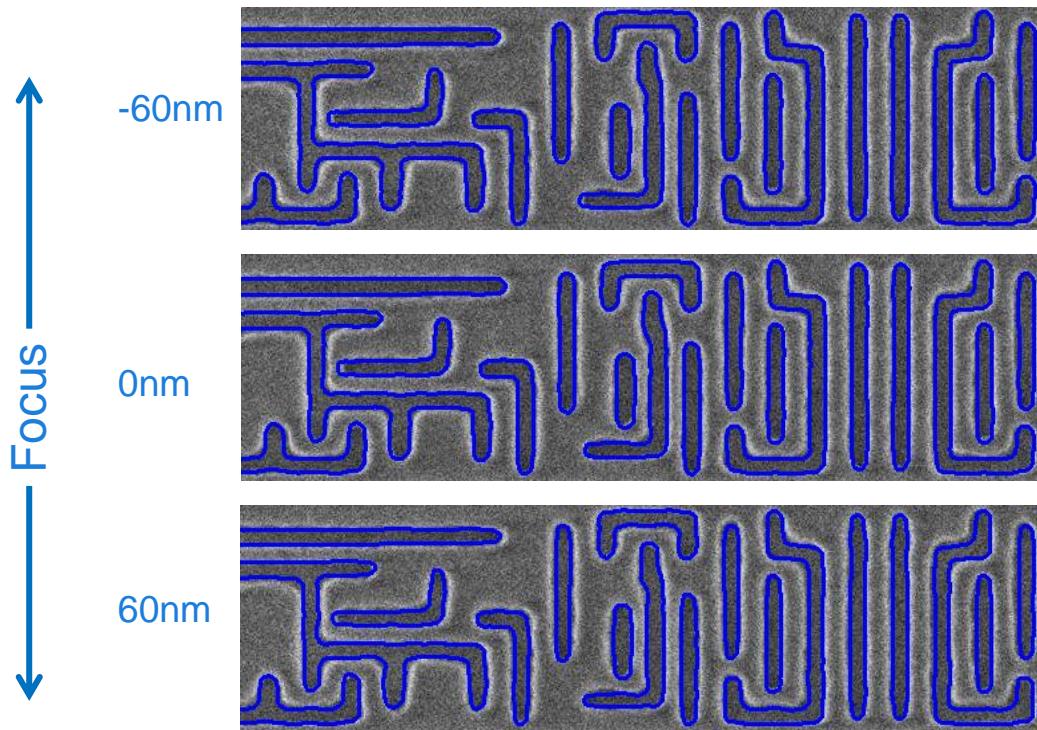
NXE:3300, 10 nm logic metal 1 layer, 45 nm pitch

ST  
life.augmented

# Model predictions confirm good printability thru focus with **ASML** Quasar and OPC

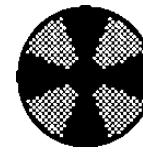
Public  
Slide 19

Calibrated Tachyon NXE M3D+ model



**Test mask with basic OPC**

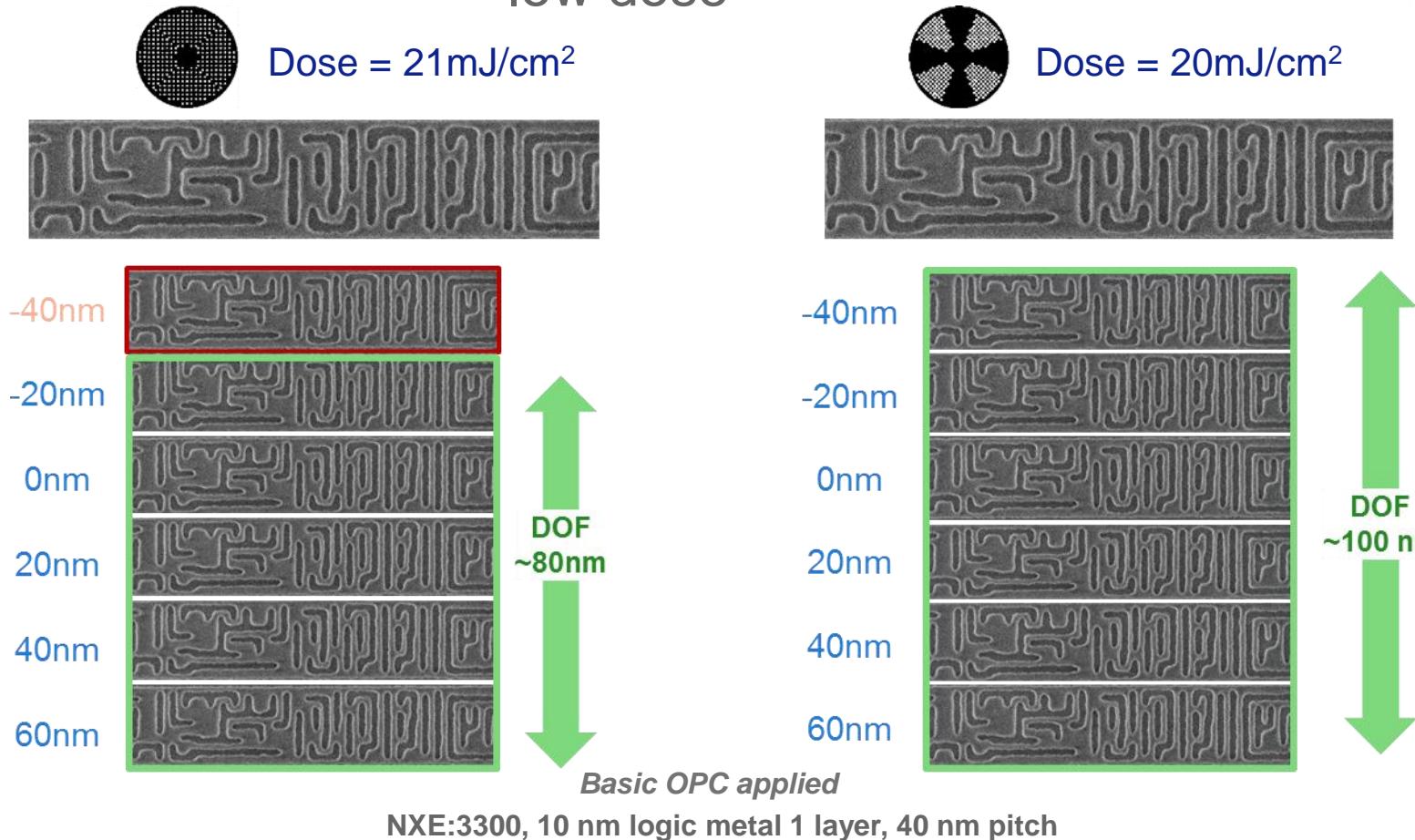
20 mJ/cm<sup>2</sup>



Early process results:  
Predicted contours (blue)  
match well SEM contours

NXE:3300, 10 nm logic metal 1 layer, 45 nm pitch

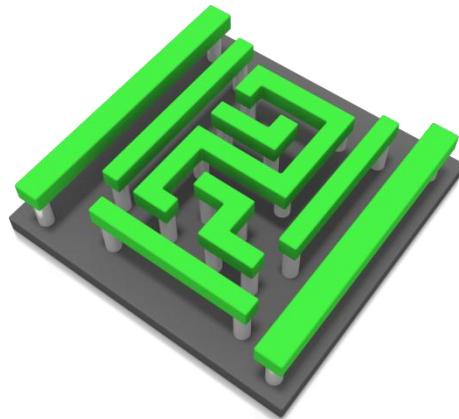
# OPC enables scaling to sub-N10 (40nm) min. pitch at low dose



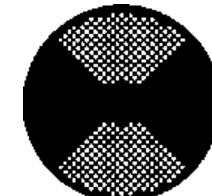
# Contents

- NXE:3300B imaging performance – Building blocks
  - *CDU, HV and through pitch performance from scanner qualification*
  - *Line end control*
- 2D random logic – 10nm node Metal 1
  - *OPC model calibration and hotspot verification*
- **Towards 7nm node logic**
- Summary and conclusions

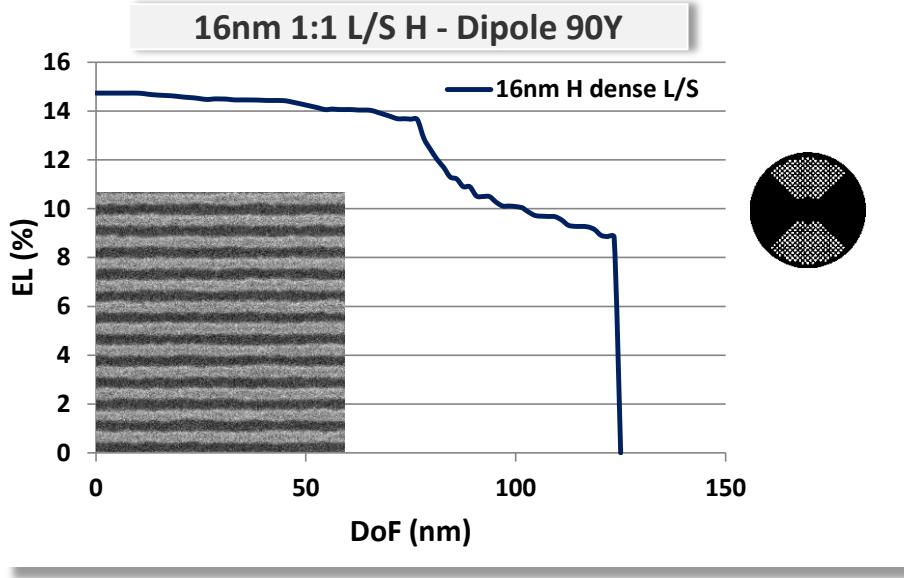
# Initial evaluation of N7 Logic M1 done on ASML's NXE:3300B using Quasar and Dipole illumination



Logic M1 – 7nm node	
Min. pitch	~ 32 – 36nm
Min. Tip-to-tip	~25-35nm
Min. Tip-to-space	~18-25nm



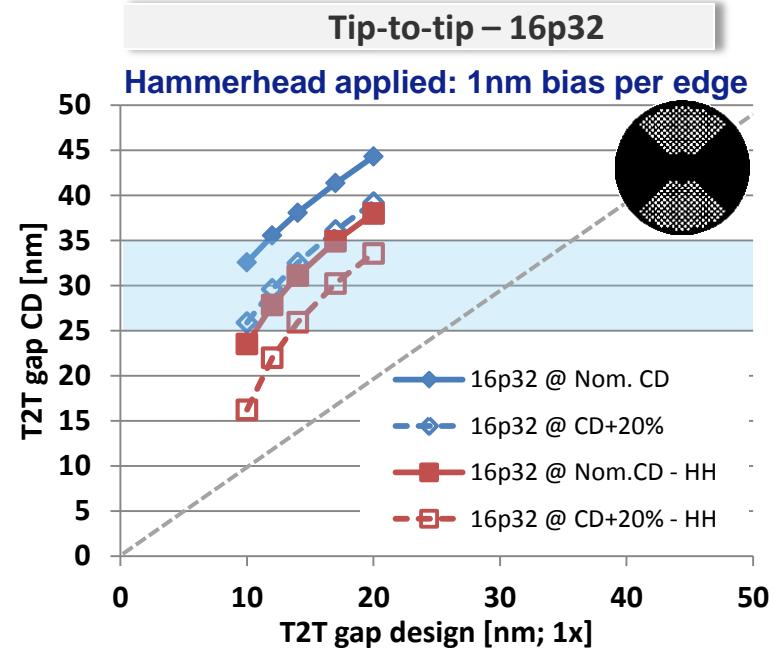
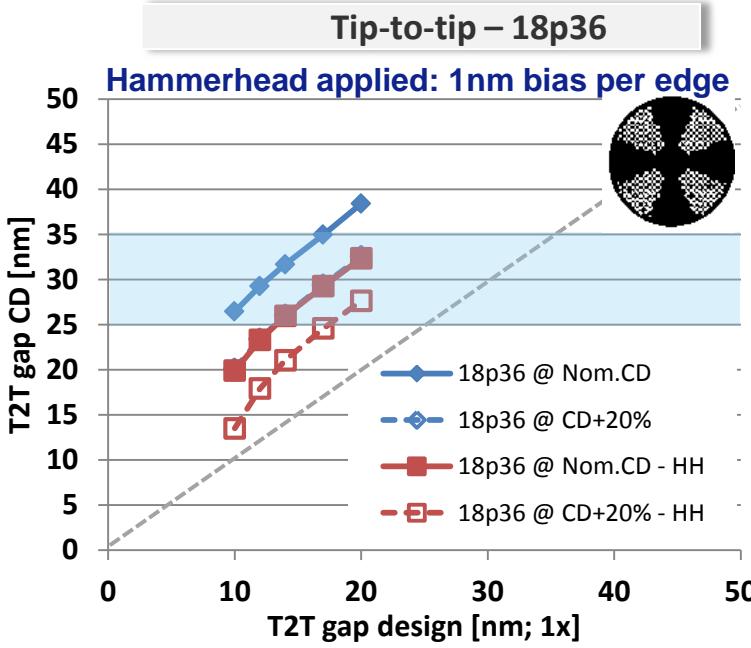
# Large PWs on NXE:3300B for minimum pitch N7 design



Dose-to-size ~ 55mJ/cm<sup>2</sup>

- Sufficient resolution and process window for N7 development
- Further resist development required to lower dose
- NOTE, no mask optimization done

Simulations show T2T ~20nm feasible for 7nm node resolution – Further optimization by means of FlexPupil

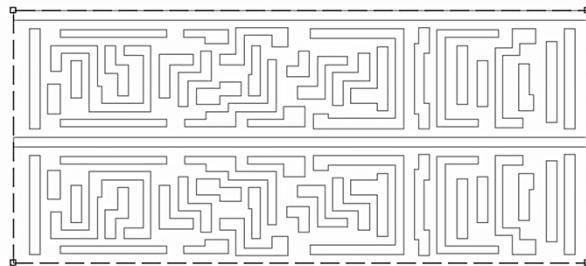


- OPC enables 20nm T2T at 36nm and 32nm pitch using std. off-axis illumination
  - MEEF ~ 1 in region of interest
- Rigorous simulation: 6nm resist blur + typical 3300 scanner

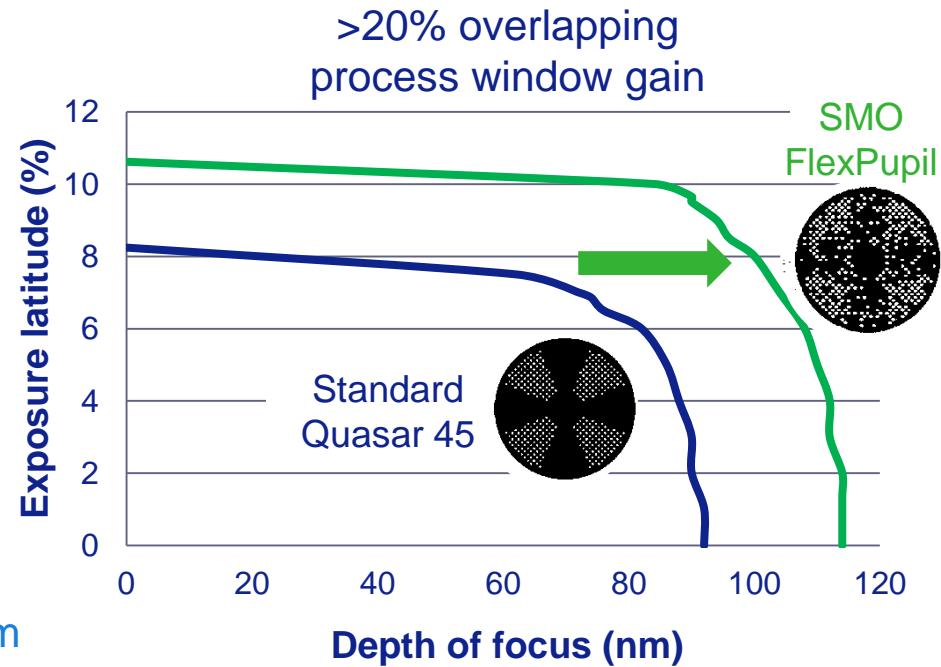
- Further optimization possible by means of FlexPupil
- 
- Rigorous simulation: 5.3nm resist blur + typical 3300 scanner

# SMO & FlexPupil can greatly improve process window

## SMO FlexPupil shape vs. best standard pupil: 7 nm node metal 1 example



- 7 nm node logic metal 1 layer
- Logic standard cells, dark field
- Tachyon NXE M3D+ model used
- NXE:3300 K1 = 0.39
- Min pitch = 32 nm, min feature 16 nm

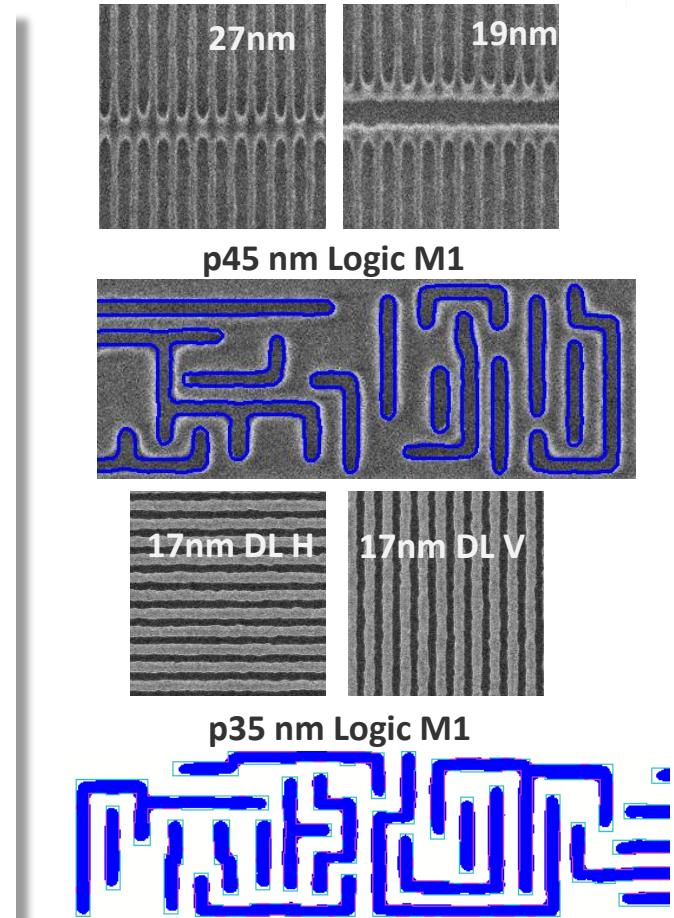


# Contents

- NXE:3300B imaging performance – Building blocks
  - *CDU, HV and through pitch performance from scanner qualification*
  - *Line end control*
- 2D random logic – 10nm node Metal 1
  - *OPC model calibration and hotspot verification*
- Towards 7nm node logic
- **Summary and conclusions**

# Summary and conclusions

- **NXE:3300B** evaluated for N10 and N7 logic performance
  - CDU, HV and proximity performance meet N10 requirements
  - Line-end performance for N10 (~45nm pitch) allows aggressive T2T and T2S design at low dose
    - T2T down to 30nm, T2S down to 20nm feasible
    - OPC required to mitigate line-end shortening and local line-end variations - Validated by rigorous simulations
  - OPC enables scaling to sub-N10 (40nm) min. pitch at <20mJ/cm<sup>2</sup> with 100nm DOF
    - Tachyon NXE OPC+ model calibrated for conventional and Quasar illumination showing good contour overlap
    - LMC correctly predicts bridge- and neck-defects through focus
  - Initial imaging performance evaluation for N7 logic started
    - 17nm HP resolution for H & V achieved with Q45
    - Rigorous simulations and calibrated Tachyon model shows '2D-style' N7 logic M1 feasible
    - SMO and FlexPupil can greatly improve process window



# Acknowledgements

**ASML**

Public

Slide 28

## Special thanks to:



- Jean Galvier



- Dan Corliss
- Chris Robinson



- Patrick Wong
- Jing Wang

### ASML demo group

- Maarten van Dorst
- Peter Rademakers
- Cynthia van den Akker

### ASML Albany

- Bart Kessels
- Brian Lee

### ASML D&E Imaging Applications

- Cristina Toma
- Natalia Davydova
- Andre van Dijk
- Frank Horsten
- Ijen van Mil
- Gijsbert Rispens
- Vadim Timoshkov

**ASML**

*Thank you for your  
attention !*